REMARKS

Prior to entry of the instant amendment, claims 1-19 and 67-73 are pending in the subject application. By the instant amendment, claims 67, 69, 72 and 73 are amended, and claims 1-19 and 71 are canceled. Claims 67, 69, 72 and 73 are independent.

Applicants appreciate the Examiner's consideration of the Information Disclosure Statement filed on February 23, 2006.

Claims 67-70, 72 and 73 are presented to the Examiner for further prosecution on the merits.

A. Introduction

In the outstanding Office action, mailed May 17, 2006, the Examiner objected to the drawings under 37 C.F.R. § 1.83(a); objected to claims 4 and 72 because of language informalities; rejected claims 1-4, 6-8, 10-13, 15-17 and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication No. 2001/0050532 to Eida et al. ("the Eida et al. reference"); rejected claims 9 and 18 under 35 U.S.C. § 103(a) as being unpatentable over the Eida et al. reference in view of U.S. Patent No. 6,329,226 to Jones et al. ("the Jones et al. reference"); rejected claims 5, 14 and 73 under 35 U.S.C. § 103(a) as being unpatentable over the Eida et al. reference in view of U.S. Patent No. 6,916,681 to Asano et al. ("the Asano et al. reference"); rejected claims 1, 67 and 68 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2005/0205868 to Yamazaki et al. ("the '868 Yamazaki et al. reference") in view of the Jones et al reference; rejected claims 69 and 71 under 35 U.S.C. § 103(a) as being unpatentable over the '868 Yamazaki et al. reference in view of the Jones et al. reference in view of the Asano et al. reference; rejected claim 70 under 35 U.S.C. § 103(a) as being unpatentable over the '868 Yamazaki et al., Jones et al. and Asano et al. references in view of U.S. Patent Publication No. 2002/0036267 to Ikeda et al. ("the Ikeda et al. reference"); and rejected claim 72 under 35 U.S.C. § 103(a) as being unpatentable over the

Eida et al. reference in view of U.S. Patent Publication No. 2002/0057055 to Yamazaki et al. ("the '055 Yamazaki et al. reference").

B. Objection to the Drawings

In the outstanding Office action, the Examiner objected to the drawings under 37 C.F.R. § 1.83(a). In particular, the Examiner asserted that the "semiconductor chip" recited in claims 1, 5, 6, 10, 13-15, 67, 69, 71 and 73 must be shown or the feature(s) canceled from the claims. Applicants respectfully traverse this objection, and respectfully submit that the feature is illustrated in the drawings as originally filed.

For example, FIGS. 2 and 4 illustrate two embodiments wherein a semiconductor chip is illustrated. In FIG. 2, the semiconductor chip is disposed on the flexible substrate 51 and underlies the protective cap 63. See also paragraph [0049] of the application as originally filed, which discloses,

> A driving unit as a switching unit, which drives the pixel unit, uses a TFT semiconductor chip. The driving unit includes a flexible substrate 51, an active layer 53 formed on an upper surface of the substrate 51 and having a source region S and a drain region D, a first insulating layer 55 and a gate electrode 57 deposited on an upper surface of the active layer 53, a second insulating layer 59 covering the surface of the gate electrode 57 and portions of the active layer 53, a source electrode 61a and a drain electrode 61b formed on the second insulating layer 59 to connect the source and the drain regions S and D of the active layer 53 and to transfer electrons and holes, and a protective cap 63 coated on surfaces of the substrate 51, the active layer 53, the second insulating layer 59, and the source and the drain electrodes 61a and 61b in order to protect the entire structure.

Similarly, FIG. 4 illustrates a semiconductor chip disposed on a first protective cap 93a and below a second protective cap 93b, as described in paragraph [0067] of the application as originally filed, which states, in part,

> The structure of a TFT-LCD 100 of FIG. 4 is similar to that of the TFT-LCD 70 of FIG. 2. However, the semiconductor device according to the second embodiment of the present invention further includes a first protective cap 93a between a substrate 81 and an active layer 83 in addition to a second protective cap 93b formed under a third insulating layer 95. Reference numerals 85, 87, 89, 91a, 91b, 95,

> 97, 99, and 101 denote a first insulating layer, a gate electrode, a second insulating layer, a source electrode, a drain electrode, a third insulating layer, a first electrode, a liquid crystal layer, and a second electrode, respectively.

In addition, it appears that this objection to the drawings substantially parallels the rejection of claims 1-19 and 67-70 under 35 U.S.C. § 112, second paragraph, that was raised by the Examiner in the Office action mailed on October 17, 2005. Applicants traversed that rejection, and note that the rejection was withdrawn in response thereto. *See the amendment filed March on 17, 2006, at section D.*

In view of the above, applicants respectfully submit that the semiconductor chip recited in the claims is already illustrated in the drawings. Therefore, applicants respectfully request that this objection be reconsidered and withdrawn.

C. Objection to Claims 4 and 72

In the outstanding Office action, the Examiner objected to claims 4 and 72 because of language informalities. In particular, the Examiner asserted that, in claim 4, the term "device" should be corrected to read "chip" and, in claim 72, the term "protective cap" should be corrected to read "capping layer." Applicants note that claim 4 has been canceled and the suggested change has been made to claim 72. Accordingly, applicants respectfully request that this objection be reconsidered and withdrawn.

D. Asserted Anticipation Rejection of Claims 1-4, 6-8, 10-13, 15-17 and 19

In the outstanding Office action, the Examiner rejected claims 1-4, 6-8, 10-13, 15-17 and 19 under 35 U.S.C. § 102(b) as being anticipated by the Eida et al. reference. By the instant amendment, claims 1-4, 6-8, 10-13, 15-17 and 19 have been canceled. Accordingly, applicants respectfully submit that this rejection is moot, and respectfully request that it be withdrawn.

E. Asserted Obviousness Rejection of Claims 9 and 18

In the outstanding Office action, the Examiner rejected claims 9 and 18 under 35 U.S.C. § 103(a) as being unpatentable over the Eida et al. reference in view of the Jones et al. reference. By the instant amendment, claims 9 and 18 have been canceled. Accordingly, applicants respectfully submit that this rejection is moot, and respectfully request that it be withdrawn.

F. Asserted Obviousness Rejection of Claims 5, 14 and 73

In the outstanding Office action, the Examiner rejected claims 5, 14 and 73 under 35 U.S.C. § 103(a) as being unpatentable over the Eida et al. reference in view of the Asano et al. reference. By the instant amendment, claims 5 and 14 have been canceled. Accordingly, applicants respectfully submit that this rejection is moot with respect to claims 5 and 14. With respect to claim 73, applicants respectfully traverse this rejection, and respectfully submit that the Examiner failed to set forth a *prima facie* case of obviousness for at least the reasons set forth below.

1) All elements

In the outstanding Office action, the Examiner asserted that feature 6 illustrated in FIG. 7 of the Eida et al. reference is equivalent to a protective material on an upper surface of the semiconductor chip. *Office action of May 17, 2006, at page 5.* Applicants respectfully disagree.

a. Structure of the semiconductor chip

Applicants respectfully submit that feature 6 is not *on* an upper surface of the transistor because it is part of the transistor. Referring to FIG. 7, feature 6 is illustrated as being an electrically insulating layer 6 that is disposed between a gate electrode 54 and a source electrode 52. That is, the electrically insulating layer is an embedded insulating layer that is required in order to electrically isolate the transistor gate electrode from the transistor

source electrode. By way of comparison, in FIG. 2 of the subject application an insulating layer 59 is illustrated between a gate electrode 57 and a source electrode 61a, and the protective cap 63 covers the source electrode 61a, the gate electrode 57 *and* the insulating layer 59. Accordingly, applicants respectfully submit that feature 6 is not on an upper surface of the semiconductor chip.

Applicants respectfully submit that the Asano et al. reference fails to provide the teachings that are missing from the Eida et al. reference. Accordingly, applicants respectfully submit that the proposed combination of the Eida et al. and Asano et al. references fails to disclose or suggest each and every element of claim 73.

b. "Protective"

Additionally, applicants respectfully submit that feature 6 is not protective. In particular, applicants note that the Eida et al. reference does not describe feature 6 as being "protective." Further, the Eida et al. reference states that feature 3, which is disposed on the electrically insulating layer 6 of the transistor, is an "intermediate insulating layer 3 . . . provided for *protecting* the TFT device." Accordingly, it is apparent that the Eida et al. reference identifies the protective features described therein, yet fails to describe feature 6 in this manner. Therefore, applicants respectfully submit that the Examiner's characterization of the Eida et al. reference is not consistent with the reference itself.

Further, applicants respectfully disagree with the Examiner's assertion that feature 704 of the Asano et al. reference is a protective cap. *Office action of May 17, 2006, at page 5.* The Asano et al. reference clearly identifies feature 704 as "an electrically insulating layer." See, e.g., col. 10, lines 1-2 of the Asano et al. reference. Further, the Asano et al. reference is replete with descriptions of protective features (see, e.g., the Abstract, which describes a protective layer 102), but does not refer to feature 704 as one of them.

Accordingly, applicants respectfully submit that the Examiner's characterization of feature 704 of a protective cap is not consistent with the Asano et al. reference itself.

2) Motivation to combine

Further, applicants respectfully submit that one of ordinary skill in the art, absent the teachings of the subject application, would not be motivated to combine the Eida et al. and Asano et al. references in the manner suggested by the Examiner. As an initial matter, applicants note that the Examiner's proffered motivation, "to further protect the chip from foreign materials," does not appear to be stated in either of Eida et al. or the Asano et al. reference. Further, the Examiner has not identified any objective support for the proffered motivation.

Moreover, the protective layer 102 described in the Asano et al. reference serves the function of a stopping layer for a chemical process. See the Asano et al. reference at, e.g., col. 4, lines 9-10. In particular, the protective layer 102 allows an adjacent layer to be chemically removed after forming a thin film device. See the Asano et al. reference at col. 5, lines 27-45. However, the Asano et al. reference provides no motivation for providing such a layer on both sides of the device, as the process described therein does not require it.

In view of the above, applicants respectfully submit that the proposed combination of the Eida et al. and Asano et al. references fails to disclose or suggest each and every element of claim 73. Therefore, applicants respectfully submit that claim 73 is allowable over the proposed combination of the Eida et al. and Asano et al. references, and respectfully request that this rejection be reconsidered and withdrawn.

G. Asserted Obviousness Rejection of Claims 1, 67 and 68

Applicants note that claim 1 has been canceled and some of the subject matter thereof has been included in claim 67, which is now presented in independent form.

In the outstanding Office action, the Examiner rejected claims 1, 67 and 68 under 35 U.S.C. § 103(a) as being unpatentable over the '868 Yamazaki et al. reference in view of the Jones et al. reference. By the instant amendment, claim 1 has been canceled. Accordingly, applicants respectfully submit that this rejection is moot with respect to claim 1. With respect to claims 67 and 68, applicants respectfully traverse this rejection, and respectfully submit that the Examiner failed to set forth a *prima facie* case of obviousness for at least the reasons set forth below.

Referring to the previous Office action of October 17, 2005, the Examiner asserted that the '868 Yamazaki et al. reference discloses a flexible substrate. *Office action of October 17, 2005, at page 2.* The Examiner now admits that the '868 Yamazaki et al. reference fails to disclose such a substrate, relying instead on the Jones et al. reference. However, applicants respectfully submit that the '868 Yamazaki et al. reference fails to disclose or suggest other features recited in claims 67 and 68, e.g., a protective cap formed on the second insulating region and on the source and drain electrodes, and between the active semiconductor element and the flexible substrate, as presently recited in claim 67.

In the outstanding Office action, the Examiner asserted that the '868 Yamazaki et al. reference discloses "a protective cap 330 (para [0142], lines 1-2) sealing the chip and an insulating region 331 (para [0142], line 6) formed on the cap." *Office action of May 17, 2006, at page 6.* Applicants respectfully disagree with this characterization of the '868 Yamazaki et al. reference.

Applicants note that that feature 330 is a silicon nitride film that serves as a passivation layer. See the '868 Yamazaki et al. reference at paragraph [0142]. However, the '868 Yamazaki et al. reference does not describe feature 330 as protective, even though the reference is replete with descriptions of "protective" features. *See '868 Yamazaki et al. reference at, e.g., paragraph [0142], which describes feature 331 as "a protective film."*

Accordingly, it is apparent that the '868 Yamazaki et al. reference identifies the protective features described therein, and fails to describe feature 330 in this manner. Therefore, applicants respectfully submit that the Examiner's characterization of the '868 Yamazaki et al. reference is not consistent with the reference itself. Moreover, while feature 331 may be described as a protective layer, '868 Yamazaki et al. reference fails to describe an insulating region formed thereon.

In view of the above, applicants respectfully submit that the '868 Yamazaki et al. reference fails to disclose or suggest each and every element of claim 67. Accordingly, claim 67, as well as claim 68 depending therefrom, are believed to be allowable over the '868 Yamazaki et al. reference. Therefore, applicants respectfully request that this rejection be reconsidered and withdrawn.

H. Asserted Obviousness Rejection of Claims 69 and 71

Applicants note that, by the instant amendment, claim 69 has been amended to incorporate the subject material of claim 71 and claim 71 has, in turn, been canceled.

In the outstanding Office action, the Examiner rejected claims 69 and 71 under 35 U.S.C. § 103(a) as being unpatentable over the '868 Yamazaki et al. reference in view of the Jones et al. reference in view of the Asano et al. reference. Applicants respectfully traverse this rejection, and respectfully submit that the Examiner failed to set forth a *prima facie* case of obviousness for at least the reasons set forth below.

Independent claim 69 recites, in part,

> a protective material surrounding the semiconductor chip, wherein the protective material is on a surface of the semiconductor chip that is adjacent to the flexible substrate and is on a surface of the semiconductor chip that is opposite the flexible substrate.

In the outstanding Office action, the Examiner asserted that the combination of the '868 Yamazaki et al. reference and the Asano et al. reference teaches these features of claim 69. Applicants respectfully disagree, and further submit that there is no motivation to

combine the '868 Yamazaki et al. and Asano et al. references in the manner proposed by the Examiner.

1) A protective material

In the outstanding Office action, the Examiner referred to the rejection of claims 1, 67 and 68 over the '868 Yamazaki et al. and Jones et al. references in rejecting claim 69 with respect to the "protective material" recited therein. That is, the Examiner asserted that feature 330 of the '868 Yamazaki et al. reference teaches the protective material recited in claim 69. Applicants respectfully disagree for the reasons set forth above in Section G, *viz.*, feature 330 is not a protective material.

2) A protective material surrounding the semiconductor chip

Further, applicants respectfully submit that neither the '868 Yamazaki et al. reference nor the Asano et al. reference, whether alone or in combination, teach a protective material surrounding the semiconductor chip, as recited in claim 69. Even assuming, *arguendo*, that feature 330 of the '868 Yamazaki et al. reference is a protective material, neither the '868 Yamazaki et al. reference nor the Asano et al. reference discloses or suggests a protective material "surrounding the semiconductor chip," as recited in claim 69.

Moreover, the Examiner asserted that the Asano et al. reference discloses, in FIG. 6, an active semiconductor element 607, 608 formed on a region of the protective material 603. However, the protective material 603 is formed of molybdenum and the electrical insulating layer 604 is formed for blocking electrical conductance. Therefore, even assuming, *arguendo*, that layer 603 is a protective layer, the Asano et al. reference fails to disclose or suggest forming the layer from any one of an ultraviolet curing resin, an X-ray curing material, an electronic beam curing material, and an ion beam curing material, as presently recited in claim 69.

3) Motivation to combine

As discussed above in Section F(2), applicants respectfully submit that one of ordinary skill in the art, absent the teachings for the present invention, would not be motivated to combine the '868 Yamazaki et al. and Asano et al. references in the manner suggested by the Examiner. The Examiner's proffered motivation, "to further protect the chip from foreign materials," does not appear to be stated in either the '868 Yamazaki et al. reference or the Asano et al. reference. Further, the Examiner has not identified any objective support for the proffered motivation.

Moreover, the protective layer 102 described in the Asano et al. reference serves the function of a stopping layer for a chemical process, allowing an adjacent layer to be chemically removed after forming a thin film device. However, the Asano et al. reference provides no motivation for providing such a layer on both sides of the device, as the process described therein does not require it.

In view of the above, applicants respectfully submit that claim 69, as well as claim 71 depending therefrom, are allowable over the proposed combination of the '868 Yamazaki et al. and Asano et al. references. Therefore, applicants respectfully request that this rejection be reconsidered and withdrawn

I. Asserted Obviousness Rejection of Claim 70

In the outstanding Office action, the Examiner rejected claim 70 under 35 U.S.C. § 103(a) as being unpatentable over the '868 Yamazaki et al., Jones et al. and Asano et al. references in view of the Ikeda et al. reference. Applicants respectfully traverse this rejection, and respectfully submit that the Examiner failed to set forth a *prima facie* case of obviousness for at least the reasons set forth below.

Claim 70 recites "wherein the tensile strength of the protective material is greater than about 30 GPa." In the outstanding Office action, the Examiner relied on the Ikeda et al.

reference to teach the recited tensile strength. Applicants respectfully submit that rejection on this basis is improper.

The Examiner asserted that a "protective cap formed of acrylic resin inherently has a tensile strength greater than about 30 GPa and a hardness greater than about 200 Brinell." However, the Examiner has not provided proper support for this inherency argument. The Examiner is obligated to present evidence that makes clear that the missing descriptive matter is *necessarily* present. The mere fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient. (MPEP § 2112, citing *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)). The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. (MPEP § 2112, citing *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Applicants respectfully submit that one of ordinary skill in the art would appreciate that an acrylic resin may be formed to have any one of a number of physical properties and, in particular, may be formed to have various strengths and hardnesses.

In view of the above, applicants respectfully submit that claim 70 is allowable over the proposed combination of references. Therefore, applicants respectfully request that this rejection be reconsidered and withdrawn.

J. Asserted Obviousness Rejection of Claim 72

In the outstanding Office action, the Examiner rejected claim 72 under 35 U.S.C. § 103(a) as being unpatentable over the Eida et al. reference in view of the '055 Yamazaki et al. reference. Applicants respectfully traverse this rejection, and respectfully submit that the Examiner failed to set forth a *prima facie* case of obviousness for at least the reasons set forth below.

1. Flexible substrate

Claim 72 recites a flexible substrate. The Examiner asserted that the '055 Yamazaki et al. reference discloses a capping layer 602 contacting a flexible substrate 601. *Office action of May 17, 2006, at page 9.* However, the Examiner has provided no basis for the assertion that substrate 601 is flexible.

Moreover, applicants respectfully submit that the Eida et al. reference also fails to disclose a flexible substrate. The Examiner asserted that the Eida et al. reference discloses a flexible substrate 1, and further asserted that the substrate 1 is formed of plastic, which is the same material being used by applicant to form a flexible substrate and, therefore, the substrate 1 is flexible. *Office action of May 17, 2006, at page 3.* Applicants respectfully disagree, and respectfully submit that this inherency argument lacks proper support.

Applicants note that one of ordinary skill in the art would appreciate that a given material may be engineered to exhibit a wide variety of properties, including flexibility or a lack thereof. For example, a plastic, metal or glass object may be flexible or not depending on, e.g., its thickness, its shape, etc. Accordingly, one of ordinary skill in the art would appreciate that a mere disclosure of a material, e.g., plastic, absent any additional details of how the material is engineered for use in a particular device, does not require that material to exhibit a particular property such as flexibility. Therefore, applicants respectfully submit that one of ordinary skill in the art would appreciate that every plastic device is not inherently flexible.

Moreover, to support an argument based on inherency, the Examiner is obligated to present evidence that makes clear that the missing descriptive matter is necessarily present. The mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient. (*In re Rijckaert*). The mere fact that a certain thing may result from a given set of circumstances is not sufficient. (*In re Robertson*). However, the Eida et al. reference does not provide the required necessary support for alleging that the substrate 1 is inherently

flexible. Accordingly, applicants respectfully submit that a flexible substrate is not taught by the proposed combination of the Eida et al. and '055 Yamazaki et al. references.

2. Capping layer

Claim 72 recites, in part "a capping layer that forms an upper surface of the driving unit and contacts the flexible substrate." Such a capping layer is illustrated in FIG. 2 of the application as originally filed, wherein a protective cap 63 comes down the sides of the TFT semiconductor chip to contact the flexible substrate 51. In the outstanding Office action, the Examiner admitted that the Eida et al. reference fails to disclose a capping layer contacting the flexible substrate. *Office action of May 17, 2006, at page 9.* Instead, the Examiner relied on the '055 Yamazaki et al. reference to teach this feature.

In particular, the Examiner asserted that the '055 Yamazaki et al. reference discloses, in FIG. 6 therein, a capping layer 602 contacting the substrate 601. However, it is clear from FIG. 6 that the capping layer does not form an upper surface of the driving unit, as recited in claim 72. Rather, feature 602 of the '055 Yamazaki et al. reference is *below* every TFT illustrated in FIG. 6.

Thus, the Examiner is relying on the Eida et al. reference for "forms an upper surface" and on the '055 Yamazaki et al. reference for "contacts the flexible substrate." This aspect of the rejection is essentially the same as the rejections of claims 5, 14 and 73 over the Eida et al. and Asano et al. references that was discussed above in Section F(2). For reasons similar to those set forth above in Section F(2), applicants respectfully submit that neither the '055 Yamazaki et al. reference nor the Eida et al. reference provides a motivation for the modifications suggested by the Examiner, *viz.*, extending the capping layer from the upper surface of the driving unit down to contact the substrate.

3. Tensile strength and hardness

Claim 72 also recites, "the capping layer has a tensile strength higher than about 30 GPa and a hardness higher than about 200 Brinell." In the outstanding Office action, the Examiner asserted that the Eida et al. reference discloses a capping layer 6 that inherently exhibits these attributes. Applicants respectfully disagree, and submit that the Examiner failed to provide the necessary support for this inherency argument for the reasons set forth above in Section I.

K. Conclusion

If the Examiner believes that additional discussions or information might advance the prosecution of the instant application, the Examiner is invited to contact the undersigned at the telephone number listed below to expedite resolution of any outstanding issues.

In view of the foregoing remarks, reconsideration of this application is earnestly solicited, and an early and favorable further action upon all pending claims is hereby requested.

Respectfully submitted,

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PETITION and DEPOSIT ACCOUNT CHARGE AUTHORIZATION

This document and any concurrently filed papers are believed to be timely. Should any extension of the term be required, applicant hereby petitions the Director for such extension and requests that any applicable petition fee be charged to Deposit Account No. 50-1645.

If fee payment is enclosed, this amount is believed to be correct. However, the Director is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-1645.

Any additional fee(s) necessary to effect the proper and timely filing of the accompanying-papers may also be charged to Deposit Account No. 50-1645.